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ARTICLE

Damage-Free Smooth-Sidewall InGaAs Nanopillar Array by Metal-Assisted Chemical Etching

Lingyu Kong,[†,‡,§,∥] Yi Song,[†,∇] Jeong Dong Kim,[†] Lan Yu,[†,∇] Daniel Wasserman,[†,○] Wai Kin Chim,[§] Sing Yang Chiam,[∥] and Xiuling Li*[,†,⊥]

[†]Department of Electrical and Computer Engineering, Micro and Nanotechnology Laboratory, Materials Research Laboratory, University of Illinois at Urbana−Champaign, Urbana, Illinois 61801, United States

[⊥]International Institute for Carbon-Neutral Energy Research (I2CNER), Kyushu University, Fukuoka 819-0395, Japan

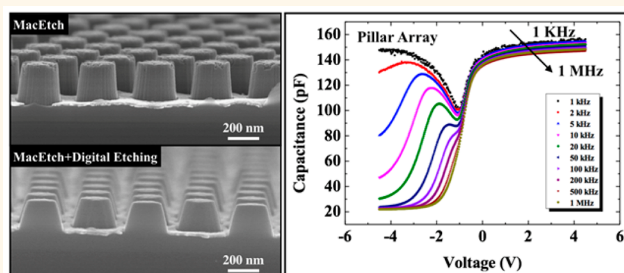
[‡]NUS Graduate School for Integrative Sciences and Engineering, National University of Singapore, 28 Medical Drive, Singapore 117456

[§]Department of Electrical and Computer Engineering, National University of Singapore, 4 Engineering Drive 3, Singapore 117583

[∥]Institute of Materials Research and Engineering, A*STAR (Agency for Science, Technology and Research), 2 Fusionopolis Way, Innovis, Singapore 138634

S *Supporting Information*

ABSTRACT: **Producing densely packed high aspect ratio $In_{0.53}Ga_{0.47}As$ nanostructures without surface damage is critical for beyond Si-CMOS nanoelectronic and optoelectronic devices. However, conventional dry etching methods are known to produce irreversible damage to III−V compound semiconductors because of the inherent high-energy ion-driven process. In this work, we demonstrate the realization of ordered, uniform, array-based $In_{0.53}Ga_{0.47}As$ pillars with diameters as small as 200 nm using the damage-free metal-assisted chemical etching (MacEtch) technology combined with the post-MacEtch digital etching smoothing. The etching mechanism of $In_xGa_{1-x}As$ is explored through the characterization of pillar morphology and porosity as a function of etching condition and indium composition. The etching behavior of $In_{0.53}Ga_{0.47}As$, in contrast to higher bandgap semiconductors (*e.g.*, Si or GaAs), can be interpreted by a Schottky barrier height model that dictates the etching mechanism constantly in the mass transport limited regime because of the low barrier height. A broader impact of this work relates to the complete elimination of surface roughness or porosity related defects, which can be prevalent byproducts of MacEtch, by post-MacEtch digital etching. Side-by-side comparison of the midgap interface state density and flat-band capacitance hysteresis of both the unprocessed planar and MacEtched pillar $In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor capacitors further confirms that the surface of the resultant pillars is as smooth and defect-free as before etching. MacEtch combined with digital etching offers a simple, room-temperature, and low-cost method for the formation of high-quality $In_{0.53}Ga_{0.47}As$ nanostructures that will potentially enable large-volume production of $In_{0.53}Ga_{0.47}As$-based devices including three-dimensional transistors and high-efficiency infrared photodetectors.**



KEYWORDS: *$In_{0.53}Ga_{0.47}As$, metal-assisted chemical etching, MacEtch, porous shell, Schottky barrier height, digital etching, MOSCAPs*

Metal-assisted chemical etching (MacEtch), as discovered by Li and Bohn in 2000,[1] is a powerful etching technique for fabricating a wide range of semiconductor micro- or nanostructures without using the conventional dry etching approaches.[2−11] The simplicity, versatility, and cost effectiveness of the method has provided the motivation to explore the use of this technique for applications in many different areas over the past two decades, including electronics,[12] optoelectronics,[13−17] biological or chemical sensors,[18] energy harvesting[19,20] and storage applications.[21] In essence, the MacEtch process involves a thin layer of noble metal (*e.g.*, Ag, Au, *etc.*) acting as a catalyst to guide and

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accelerate the etching process in a solution that consists of an oxidant for semiconductor oxidation reaction and an acid for oxidized material dissolution reaction. Under controlled conditions, the continuous repetition of such an oxidation (carrier generation and injection) and oxide dissolution (mass transport) cycle[6,22,23] allows for anisotropic etching of the semiconductor material directly underneath the catalyst metal, leaving behind semiconductor structures that are complementary to the metal catalyst pattern.

The current state of research in this field has been primarily focused on the etching of Si,[2,3] Ge,[24] and SiGe heterostructures or alloys.[25,26] The etching of III−V compound semiconductors, such as GaAs,[10,13,16] InP,[11,12] GaN,[27] and GaP,[28] has also been explored recently. However, unlike the conventional MacEtch of Si in HF/H_2O_2, due to the compound material nature, the resultant etching morphology and profile of different compound semiconductors are distinct. Moreover, the etching mechanism, etching conditions (*i.e.*, temperature or UV light assisted), and the choice of acid and oxidant pairs vary as well. Even though the MacEtch technique is proven to be capable of processing medium or wide bandgap optoelectronic materials as mentioned above, employing such an etching technique on narrow bandgap III−V semiconductors, such as $In_{0.53}Ga_{0.47}As$ (∼0.74 eV) and InAs (∼0.35 eV), has yet to be established.

$In_xGa_{1-x}As$, as one of the crucial ternary alloys, has emerged as a promising channel material candidate for next-generation high-speed and low-power nanoelectronics and optoelectronics involving metal-oxide-semiconductor field-effect transistors (MOSFETs) or short-wavelength infrared (IR),[29−32] owing to its high carrier mobility and tunable bandgap energy. To further enhance the $In_{0.53}Ga_{0.47}As$-based electronic and optoelectronic device performance, including increasing the on-current and decreasing off-current per chip surface area for MOSFETs or reducing the dark current and improving the quantum efficiency for IR photodetectors, the development of techniques to fabricate three-dimensional (3D), densely packed $In_{0.53}Ga_{0.47}As$ nanostructures is essential.[33]

So far, conventional fabrication techniques for $In_{0.53}Ga_{0.47}As$ nanostructures require either bottom-up crystal growth processes, such as selective-area epitaxy (SAE) or direct epitaxy,[34,35] or top-down approaches, such as reactive-ion etching (RIE) or inductively coupled plasma-reactive ion etching (ICP-RIE).[30,36] The epitaxial approach demands a sophisticated growth system with the capability of handling toxic gases and high-vacuum and high-temperature reactions. For the dry etching techniques, the high-energy ions can introduce severe irreversible damages to the semiconductor crystal structure and surface morphology due to the difficulty of maintaining the surface stoichiometry by annealing in compound semiconductors.[37] Narrow bandgap compound semiconductors are especially susceptible to dry etch damages. However, MacEtch, as an alternative approach, could avoid the above-mentioned common issues associated with both the commonly used top-down and bottom-up approaches. It could eliminate the dry etching-induced surface damages,[38] and the undulating sidewall or nonvertical etching profile,[30,36,39] that have undesirable effect on device characteristics. It is well-known that a good MOS interface quality demands a smooth surface with minimum dry etching damages. Recently, a single high aspect ratio $In_{0.53}Ga_{0.47}As$ pillar-based transistor, fabricated using ICP-RIE and subsequently smoothed by multiple cycles of digital etching, was demonstrated with impressive performance.[36] However, the density of $In_{0.53}Ga_{0.47}As$ pillars fabricated using this technique appears to be low. Moreover, the sidewall of the nanowire is not quite vertical. In addition, the bottom trenching profile could adversely affect the device process integration. In general, the high temperature involved in post-dry etching annealing process could potentially create high-thermal budget-related compatibility issues for device application.

In this work, we demonstrate the fabrication of ordered $In_{0.53}Ga_{0.47}As$ pillars array with damage-free sidewall surfaces using MacEtch. Vertical etch rate, etching morphology, and porous shell thickness as a function of etching solution parameters, including HF:DI water ratio, oxidant concentration, are systematically investigated and compared with GaAs and InAs MacEtch. It is found that the $In_{0.53}Ga_{0.47}As$ MacEtch is confined in the mass transport limited regime, that is, the rate-determining step is the oxide removal, regardless of variation in etching solution parameters. This results in slow etch rate and the formation of the porous shell. $In_{0.53}Ga_{0.47}As$ pillars with high verticality and minimized porous shells are achieved under controlled etching condition. To realize $In_{0.53}Ga_{0.47}As$ pillars with smooth sidewall surfaces, an optimized digital etching process is developed to completely remove the porous shell as well as surface grooves associated with the edge roughness of the patterned catalyst metal film. $In_{0.53}Ga_{0.47}As$ pillar-based MOS capacitors (MOSCAPs) are then fabricated to confirm the quality of the etched surface. Comparable midgap interface state density (∼1.9−2.2 × 10^{12} cm^{-2} eV^{-1}) and flat-band capacitance hysteresis (∼150−175 mV) are extracted from the capacitance−voltage (C−V) profiles of both pillar and planar (control) $In_{0.53}Ga_{0.47}As$ MOSCAPs. This indicates that the sidewalls of the resultant pillars are as trap-free as the planar $In_{0.53}Ga_{0.47}As$ epitaxial film, confirming the damage-free quality of the pillar array produced by MacEtch and subsequent digital etching.

RESULTS AND DISCUSSION

Figure 1 shows a 45°-tilt view scanning electron microscopy (SEM) image of an ordered $In_{0.53}Ga_{0.47}As$ pillar array (patterned by nanosphere lithography technique using ∼390 nm diameter nanospheres) resulted from MacEtch in a solution consisting of 14.2 M HF and 3.2 mM $KMnO_4$ for 8 min. The inset shows a higher magnification cross-section view of the same sample. The Au catalyst, $In_{0.53}Ga_{0.47}As$ pillars, $In_{0.53}Ga_{0.47}As$ epitaxial layer and the n-type InP substrate can be clearly distinguished.

The observation of the continuous Au catalyst mesh at the bottom of the pillars (*i.e.*, the etch front) is inherent to the MacEtch catalyst nature, just as reported previously in many other MacEtch cases, such as Si,[5,9] GaAs,[13,16] *etc.* The vertical grooves appearing on the sidewalls of the pillars are attributed to the edge roughness of the Au mesh pattern, which was engraved onto the sidewalls of the pillars as the Au mesh descended into the semiconductor during MacEtch. However, compared to GaAs, the $In_{0.53}Ga_{0.47}As$ MacEtch shows a significantly slower etch rate (see details in Figure 2 below) and lateral etching-induced nonvertical sidewalls. These distinct etching behaviors could be attributed to the different properties of $In_{0.53}Ga_{0.47}As$, such as carrier mobility, band alignment with respect to the redox potential of the oxidant and electron affinity. Therefore, to better understand the etching mechanism of $In_{0.53}Ga_{0.47}As$ and to optimize the etching process to produce surfaces with excellent quality, including better sidewall verticality, surface smoothness, and porosity control, a

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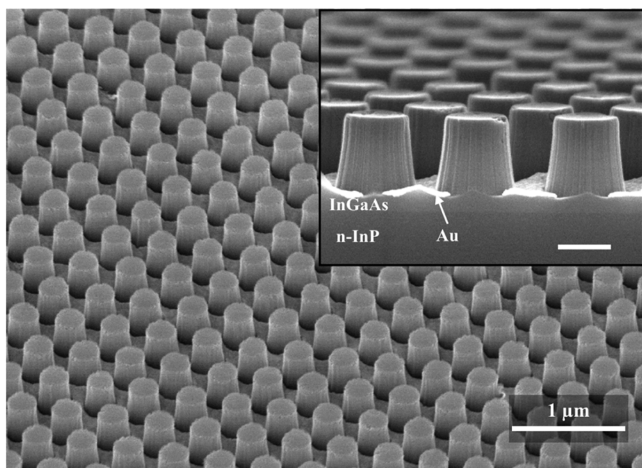

Figure 1. SEM micrograph (45°-tilt view) of an array of $In_{0.53}Ga_{0.47}As$ pillars formed from an epitaxially grown ∼500 nm-thick $In_{0.53}Ga_{0.47}As$ layer on n-InP by MacEtch in a solution of 14.2 M HF and 3.2 mM $KMnO_4$ for 8 min. The inset shows a higher magnification cross-section view of the same sample, where the scale bar represents 200 nm. The $In_{0.53}Ga_{0.47}As$ epitaxial layer (lighter contrast) and the n-InP substrate can be clearly distinguished in the inset, and the sidewall roughness of the $In_{0.53}Ga_{0.47}As$ pillars results from the edge roughness of the Au catalyst pattern.

systematic study was carried out to investigate the effect of (1) HF concentration, (2) $KMnO_4$ concentration, and (3) indium composition on etch rate, nanostructure etch profile, and porosity.

Note that the catalytic etching does not occur at the Au/InP interface, as a thick and insoluble oxide layer formed at the interface, effectively blocking the carrier transport at the etch front, as previously reported.[11] Thus, if the vertical descending of the Au catalyst mesh reaches the InP substrate, further catalytic dissolution of $In_{0.53}Ga_{0.47}As$ pillars will occur laterally near the Au/InP interface, which eventually results in pillars with "inverted" sidewall profile, as shown in Figure S1 (Supporting Information). To avoid this issue, the etching duration was precisely calibrated to prevent the catalyst from reaching the InP substrate for all experiments in this report.

Effect of HF Concentration on $In_{0.53}Ga_{0.47}As$ MacEtch. Figure 2a shows the $In_{0.53}Ga_{0.47}As$ pillar vertical etch rate (black dashed line with rectangle symbols) and sidewall angle (blue dashed line with circle symbols) as a function of HF concentration, at room-temperature with constant oxidant concentration of 5.3 mM $KMnO_4$. All data points represent measurements obtained from sample sets of 20 pillars, while the error bars represent the standard deviation from the average value. The vertical etch rate initially increases as the concentration of HF is increased, indicating that the dissolution rate of the oxidized material is the rate-determining step and the etching is in the mass transport limited regime.[6,22,23] However, beyond a critical HF concentration (19 M), the vertical etch rate is dramatically reduced. One possible reason for the rate drop is the reduction of DI water in the solution with increasing HF concentration, as the total volume was kept constant for all data points in this set of experiments. DI water was reported to facilitate the mass transport at the catalyst/semiconductor interface by playing the role of surfactant and allowing HF to access the oxidized material.[13] Therefore, the etch rate cannot be monotonically accelerated or even leveled off by continuously increasing the HF concentration, as the ratio of HF and DI water needs to be considered as well. Note that the accuracy of the height measurement is limited by the shape of the pillars which are partially deformed (Figure S2d).

While the etch rate is increased from ∼20−50 nm/min with increasing HF concentration, the sidewall verticality (blue dashed line with rectangle symbols in Figure 2a) continues to improve from 83° to 87°, indicating that the sidewall angle of pillars becomes more vertical as the etch rate is increased. The corresponding cross-section SEM micrographs of $In_{0.53}Ga_{0.47}As$ pillars array etched at different HF concentration conditions are shown in Figure S2a−c. For comparison, similar etch conditions resulted in etch rate of 118 ± 10 nm/min for GaAs of similar doping concentration.[16] The slow etch rate of $In_{0.53}Ga_{0.47}As$ allows the already formed pillars to experience lateral chemical etching as MacEtch proceeds downward, resulting in the nonideal vertical profiles.

At HF concentrations beyond 19 M where etch rate reduces significantly, the morphology of $In_{0.53}Ga_{0.47}As$ pillars (Figure S2d) is no longer well-defined, with curved sidewalls or bent pillars, indicating that pillars are not as solid as under lower HF etching conditions. Moreover, a thick porous layer underneath the Au catalyst is observed, which extends from the interface all the way to the inside of $In_{0.53}Ga_{0.47}As$ pillars, suggesting that the pillars become completely porous under this etching condition. Unlike MacEtch of Si,[40,41] there is no porous layer formed at

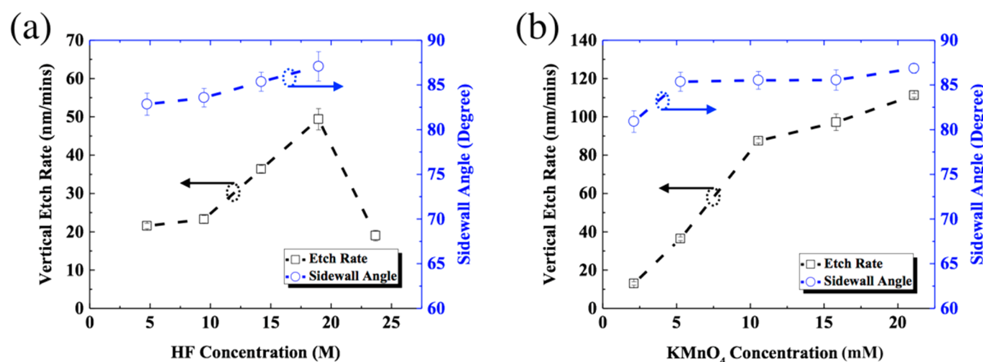

Figure 2. Plots of average measured vertical etch rate (black dashed line with rectangle symbols) and $In_{0.53}Ga_{0.47}As$ pillar sidewall angle (blue dashed line with circle symbols) as a function of (a) HF concentration (at 5.3 mM of $KMnO_4$) and (b) $KMnO_4$ concentration (at 14.2 M of HF). Each data point represents average vertical etch rate obtained from sample sets of 20 pillars, while error bars represent standard deviation from the average value.

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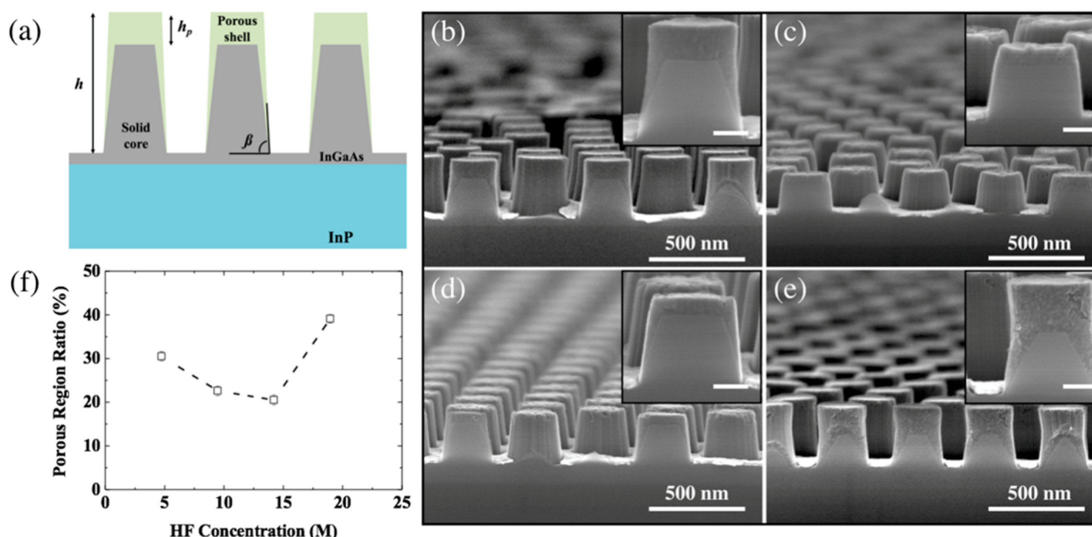

Figure 3. (a) Schematic diagram of the $In_{0.53}Ga_{0.47}As$ pillar profile after MacEtch with parameters of sidewall angle β, pillar height h, and porous shell height h_p used for describing the etching profile. Cross-section SEM micrographs of $In_{0.53}Ga_{0.47}As$ pillar array (patterned by 390 nm nanospheres) etched in solutions consisting of (b) 4.7 M, (c) 9.5 M, (d) 14.2 M, (e) 19 M HF and constant 5.3 mM $KMnO_4$ for 7, 5, 5, and 5 min, respectively. The inset shows a higher magnification view of the same sample with 100 nm scale bar. The ratio of $In_{0.53}Ga_{0.47}As$ porous shell (rough portion) to solid core (smooth portion) is reliant on the etching condition. (f) Quantification of porosity region ratio as a function of HF at a fixed $KMnO_4$ concertation of 5.3 mM.

the interface between Au and $In_{0.53}Ga_{0.47}As$ for all etching conditions except under the highest HF concentration.

The observed variation in sidewall angles is undoubtedly affected by the competing etching process of carrier generation and mass transport. When mass transport of etchants and byproducts removal are the rate limiting steps, unconsumed charges out-diffuse from the Au-$In_{0.53}Ga_{0.47}As$ interface to the $In_{0.53}Ga_{0.47}As$ pillars. As a result, spatially nonspecific chemical etching takes place, which not only impacts the lateral etch rate (thus sidewall angle) but also influences the porosity of the etched pillars. The cross-section of completely porous pillars, shown in the inset of Figure S2d, provides clear evidence that such chemical etching starts to dominate if the HF concentration is too high. As MacEtch proceeds, further generation of charges at the etch front will find the shortest pathway to diffuse (*i.e.*, $In_{0.53}Ga_{0.47}As$ epitaxial layer underneath the Au catalyst) and lead to the formation of a thick layer of porous $In_{0.53}Ga_{0.47}As$ underneath the Au catalyst, which is undesirable for device applications.

Effect of $KMnO_4$ Concentration on $In_{0.53}Ga_{0.47}As$ MacEtch. Figure 2b shows the average vertical etch rate (black dashed line with rectangle symbols) and $In_{0.53}Ga_{0.47}As$ pillar sidewall angle (blue dashed line with circle symbols) as a function of $KMnO_4$ oxidant concentration, at room-temperature with a constant 14.2 M HF concentration. It can be seen that the etch rate increases linearly as a function of oxidant concentration, and the sidewall verticality profile improves. However, as the oxidant concentration increases beyond 10.6 mM, the slope of the etch rate curve reduces. This can be explained by the etching mechanism since as the carrier generation rate exceeds the mass transport rate at the specified HF concentration, the etch rate becomes limited by the removal of the oxidized materials and is less sensitive to oxidant concentration. This further implies that the etching condition with higher oxidant concentration is not recommended, as it could increase the risk of porosity in the resultant nanostructures. Moreover, once the etch rate increase starts to level off, the improvement of pillar sidewall verticality becomes negligible. The corresponding cross-section SEM images showing the sidewall verticality are shown in Figure S3a−d.

Effect of HF and Oxidant Concentration on Porosity Control. As shown in Figure S3a, where the lowest oxidant concentration was employed, although the majority portion of the $In_{0.53}Ga_{0.47}As$ is solid (the pillar core has the same contrast as the epitaxial $In_{0.53}Ga_{0.47}As$ layer underneath), a small portion of porous layer on top of the pillars can be clearly distinguished. Compared to the optimized etching condition reported for GaAs without formation of porous layer,[13] the oxidant concentration for $In_{0.53}Ga_{0.47}As$ in this experiment is five times weaker. The formation of a porous layer even at extremely low oxidant condition indicates that for fixed acid concentration and pattern size, tuning the concentration of oxidant is not able to move the etching mechanism from the mass transport limited regime to the charge transport limited regime. This observation is different from MacEtch of other semiconductors, including Si[42] and GaAs,[13] and the fundamental reason behind this difference will be discussed next.

To investigate the influence of etching conditions on porosity, the cross sections of the $In_{0.53}Ga_{0.47}As$ pillars need to be compared. Geometric parameters of the etching profile are defined in Figure 3a, including maximum pillar height (h), sidewall angle (β), and top porous layer height (h_p). Note that 390 nm diameter closely packed nanospheres were used for patterning to allow a higher chance of cleaving the pillars through the center for cross-section view. The sidewall angle was measured with reference to the surface of the porous pillars.

Figure 3b−e show the etching profiles of the $In_{0.53}Ga_{0.47}As$ pillar arrays under the specified etching conditions, and the insets show higher magnification views of the respective samples. Note that the etching duration was designed to leave a reasonable thickness of nonporous $In_{0.53}Ga_{0.47}As$ epitaxial layer to ensure accurate porosity quantification. It is

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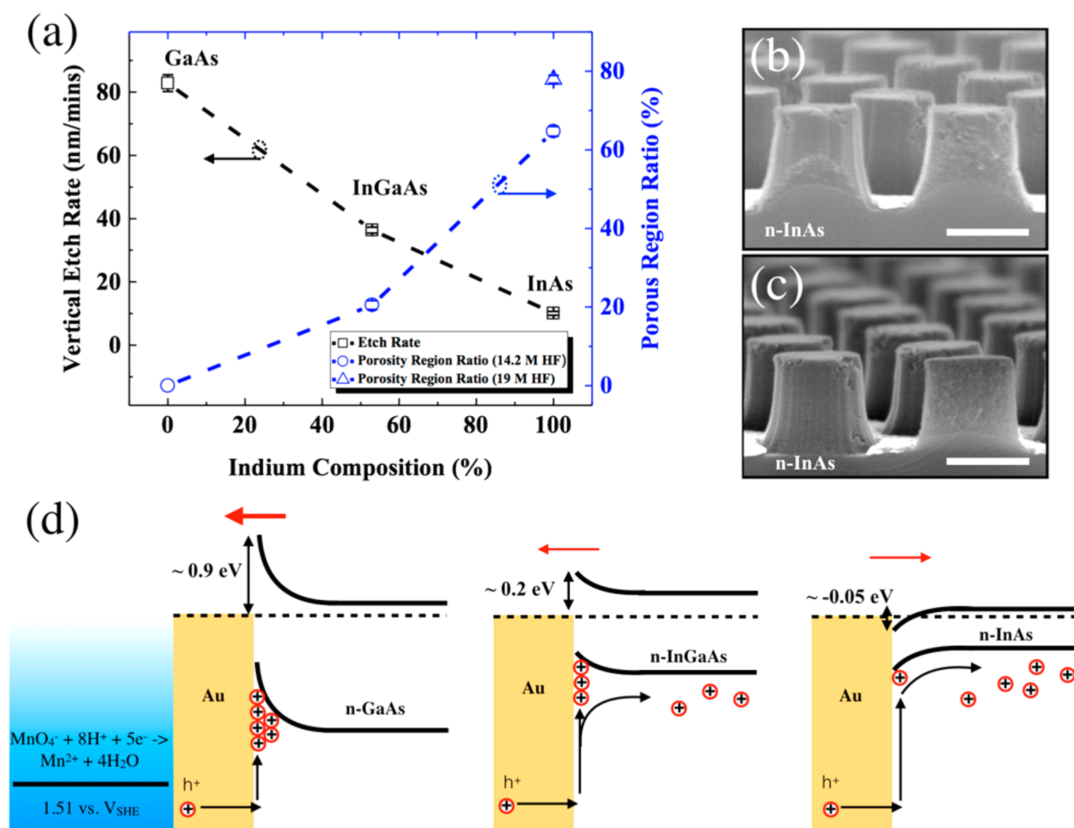

Figure 4. (a) Quantification of vertical etch rate (black dashed line with rectangle symbols) and porous region ratio (blue dashed line with circle symbols) as a function of indium composition in solutions of constant 5.3 mM $KMnO_4$ and varying amount of HF. Cross-section SEM micrographs of InAs pillar array (patterned by 390 nm nanospheres) etched in solutions of (b) 14.2 M HF or (c) 19 M HF and constant 5.3 mM $KMnO_4$ for 20 min, with scale bars of 200 nm. (d) Schematic of reduction potential of $KMnO_4$ relative to the standard hydrogen electrode (V_{SHE}) and band diagrams of the Au/n-GaAs, Au/n-$In_{0.53}Ga_{0.47}As$, and Au/n-InAs interfaces. The red arrows indicate the direction of the interface electric field. See text for details.

worth mentioning that even though the etching durations are different for each condition, the evolution of the porosity profile only depends on the variation of HF or $KMnO_4$ concentration and is invariant with the etching duration, as clearly demonstrated in Figure S4. The porous region ratio, which is defined as the ratio of the top porous layer height (h_p) to the maximum pillar height (h), as a function of HF (4.7 to 19 M) and constant 5.3 mM $KMnO_4$ concentration is shown in Figure 3f. This height ratio,h_p/h, adequately represents the porosity in the $In_{0.53}Ga_{0.47}As$ pillars without considering the sidewalls, as the porous structure thickness on the sidewalls is directly correlated to the thickness of the top porous layer. It can be observed that the lowest porous region ratio is achieved in an etching solution of 14.2 M HF and 5.3 mM $KMnO_4$. Any variation in the HF concentration away from this condition results in worse porosity. The higher porous region ratio at lower HF concentration trend from 4.7 M to 14.2 M of HF indicates that the etching mechanism is limited by mass transport. Interestingly, as the HF concentration increases from 14.2 to 19 M, the porosity become worse as well, implying that the etching remained in the mass transport limited regime for the entire HF concentration range studied here. Combining all the phenomena observed so far, we can conclude that the etching of $In_{0.53}Ga_{0.47}As$ operates in a different regime as compared to other semiconductors, such as Si[42] or GaAs,[13] as far as the catalytic etching at the Au/$In_{0.53}Ga_{0.47}As$ interface and chemical etching at the surface of the $In_{0.53}Ga_{0.47}As$ pillar are concerned. Essentially, the unconsumed charges are constantly generated at the etch front and out-diffuse from the interface to the $In_{0.53}Ga_{0.47}As$ pillars, to remotely catalyze the chemical etching of $In_{0.53}Ga_{0.47}As$, and thus resulting in the porous shell. Even though the etch rate at the Au/$In_{0.53}Ga_{0.47}As$ interface could be enhanced by a higher concentration of HF, a higher concentration of HF could also enhance the remote-catalyzed chemical etch rate of $In_{0.53}Ga_{0.47}As$ that undesirably accelerates the porous layer formation.[43] Thus, to produce $In_{0.53}Ga_{0.47}As$ pillars with vertical sidewalls and minimum porosity, the etching conditions need to be optimized to balance both the direct MacEtch and remote-catalyzed chemical etch rates. In this study, the optimized HF concentration is shown to be 14.2 M.

The effects of oxidant concentration and temperature on porosity were also investigated. It can be seen in Figure S5, an etching solution with higher oxidant concentration generally results in worse porosity. Etching under lower temperature, in an attempt to slow down the remote-catalyzed chemical etching, showed no improvement in porosity control, as demonstrated in Figure S6. A wider temperature range could be explored further in future work, but it appears unlikely to shift the balance between carrier transport and mass transport for this material. In addition, the use of porous Au catalyst[23] and nanoimprinting[22] techniques were found to enhance the mass transport for Si MacEtch of submicron or micron size features. However, these approaches are unlikely to help significantly in

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the case of $In_{0.53}Ga_{0.47}As$ because the pattern size here is already sufficiently small.

Effect of Indium Composition on Etching Profile. The experimental results in the previous sections indicate that the MacEtch of $In_{0.53}Ga_{0.47}As$ always remains in the mass transport limited regime regardless of the etching conditions employed, which is in contrast to that of GaAs. To better understand the governing factors that cause such differences, the trends of etch rate, etching profile, and porous region ratio as a function of indium composition are studied. In this experiment, GaAs (n-type, 1×10^{18} cm^{-3}), InAs (n-type, $1-3 \times 10^{18}$ cm^{-3}), and $In_{0.53}Ga_{0.47}As$ (n-type, $\sim 3 \times 10^{16}$ cm^{-3}) were used. The samples were patterned by nanosphere lithography using 390 nm diameter nanospheres and subsequently Au-MacEtched using the optimized etching condition for $In_{0.53}Ga_{0.47}As$ (*i.e.*, 14.2 M HF and 5.3 mM $KMnO_4$). An extra data point for InAs, etched in 19 M HF and 5.3 mM $KMnO_4$, was also included to investigate the InAs porosity variation as a function of HF concentration.

Figure 4a shows the plot of the etch rate (black dashed line with rectangle symbols) and porous region ratio (blue dashed line with circle symbols) as a function of indium composition. The vertical etch rate reduces and porosity increases as the indium composition increases. Compared to that of GaAs, the etch rate of $In_{0.53}Ga_{0.47}As$ and InAs under the same condition is smaller by roughly two and five times, respectively.[13,16] Overall, the trends of etch rate, etching profile, and porous region ratio for InAs as a function of HF concentration are similar to those of $In_{0.53}Ga_{0.47}As$, but the porosity for InAs is much worse. The porous region ratio for InAs pillars is roughly 65 and 80% as the concentration of HF is increased from 14.2 to 19 M, as shown in Figure 4b,c. In contrast, GaAs pillars show minimal (if any) porous layer generation either on the sidewall or on the pillar top under identical etch condition, as shown in Figure S7.

We now discuss the possible governing factors, such as different doping concentration, carrier mobility, bandgap energy, and electron affinity, that could determine the etching behavior of $In_xGa_{1-x}As$ as a function of indium composition (x).

We first examine the effect of the large difference in electron affinity that results in distinct Schottky barrier heights between Au and n-GaAs, n-$In_{0.53}Ga_{0.47}As$, and n-InAs. The interface electric field generated by the barrier height could significantly affect the charge-transfer process during MacEtch.[44] For compound semiconductors, including GaAs, $In_{0.53}Ga_{0.47}As$, and InAs, surface or interfacial defect states can pin the Fermi level (E_F) of the contacting metal at a fixed position in the bandgap.[45−47] For GaAs, it is well-known that E_F of the contacting metal is pinned at ∼0.9 eV below the GaAs conduction band.[45] Thus, the actual Schottky barrier height (∼0.9 eV) is mostly determined from this pinning effect rather than by the work function of metal.[45] Similarly for $In_{0.53}Ga_{0.47}As$, the Schottky barrier height due to Fermi level pining effect is reported to be ∼0.2 eV.[48] However, in the case of InAs, it is known that the E_F of the contacting metal is pinned above the conduction band edge of InAs, which results in the energy bands bending downward to form an ohmic contact.[47,48] The schematic in Figure 4d illustrates the reduction potential of $KMnO_4$ relative to V_{SHE} and the band diagrams at the metal−semiconductor junctions for Au/n-GaAs, Au/n-$In_{0.53}Ga_{0.47}As$, and Au/n-InAs. During the etching process, the generated carriers (h^+) oxidize GaAs, $In_{0.53}Ga_{0.47}As$, and InAs, owing to the higher redox potential of $KMnO_4$ with respect to valence band edge or ionization potential of these three semiconductors. The distribution of carriers varies significantly because of the different electric field strength induced by the respective Schottky barrier height at the metal−semiconductor junction. For Au/n-GaAs with large Schottky barriers height (∼0.9 eV), the resultant band bending can trap positive charges at the Au/n-GaAs interface. In comparison, for Au/n-$In_{0.53}Ga_{0.47}As$, the band bending from the depletion field is smaller in magnitude, and thus the trapping efficiency is expected to be lower. This allows the escape of carriers into the bulk. Finally, in the case of Au/n-InAs, the energy band bending generates a field that is in an opposite direction. This can cause the drift of injected holes into the bulk of InAs, which will result in a significant reduction of the oxidizing carriers at the Au/n-InAs interface. Therefore, under the same etching condition (*i.e.*, 14.2 M HF and 5.3 mM $KMnO_4$), GaAs exhibits the fastest vertical etch rate with minimal (if any) porous layer formation (Figure S7), as compared to $In_{0.53}Ga_{0.47}As$ or InAs. The faster etch rate makes possible the transition of GaAs MacEtch from the mass transport limited regime to the carrier generation limited regime through the HF and $KMnO_4$ concentration variation.[10,13] For $In_{0.53}Ga_{0.47}As$, since there are less injected holes at the Au/semiconductor interface, the vertical etch rate is slower. The escaped carriers from the interface can end up at the sidewalls of the $In_{0.53}Ga_{0.47}As$ pillars, resulting in the porous layer formation as observed. For InAs, the drift of injected hole carriers away from the Au/n-InAs interface resulted in a significant slow down of the etching rate and enhanced the porosity formation. These experimental results provide clear evidence to show that a lower Schottky barrier height affected the interface field in the semiconductor that restricted the etching rate of $In_{0.53}Ga_{0.47}As$ and InAs, thus keeping the MacEtch process in the mass transport limited regime. This is true even at extremely low oxidant concentration, as the carriers are not confined to the interface causing a slow down in the vertical etching speed and enhanced porosity formation away from the etching front. Thus, the Schottky barrier height is an important indication of the interface field that determines the rate-limiting step for the MacEtch of narrow bandgap compound semiconductors. High etch rate and low porosity can typically be achieved only for semiconductors with a significant Schottky barrier height, and the correct selection of the etching conditions can then confine the etching to be in the charge transport limited regime.

We note that the $In_{0.53}Ga_{0.47}As$ sample used for this study has a lower doping concentration ($\sim 3 \times 10^{16}$ cm^{-3}) than GaAs (1×10^{18} cm^{-3}) and InAs ($1-3 \times 10^{18}$ cm^{-3}). However, it is known that the Fermi level pinning in the midgap for (001) $In_{0.53}Ga_{0.47}As$ makes the Schottky barrier height almost independently of the dopant concentration in the bulk.[46] Therefore, our analysis above based on the Schottky barrier model (Figure 4d) does not change despite of the doping level difference. Similarly, the Fermi level in n-type Si is known to be pinned below the conduction band. In the MacEtch process, the depletion field that traps holes at the Au/n-Si interface remains a similar strength for a wide range of doping levels. Correspondingly, as reported in the literature, n-type Si with different doping concentration (varied from $\sim 8 \times 10^{19}$ cm^{-3} to 5×10^{15} cm^{-3}) exhibited a similar etch rate.[44] For GaAs, the MacEtch rate was comparable for both highly doped n-type and semi-insulating samples, without formation of any obvious porous layer.[13] The carrier mobility can also be excluded, as the difference in the hole mobility for the three semiconductors is

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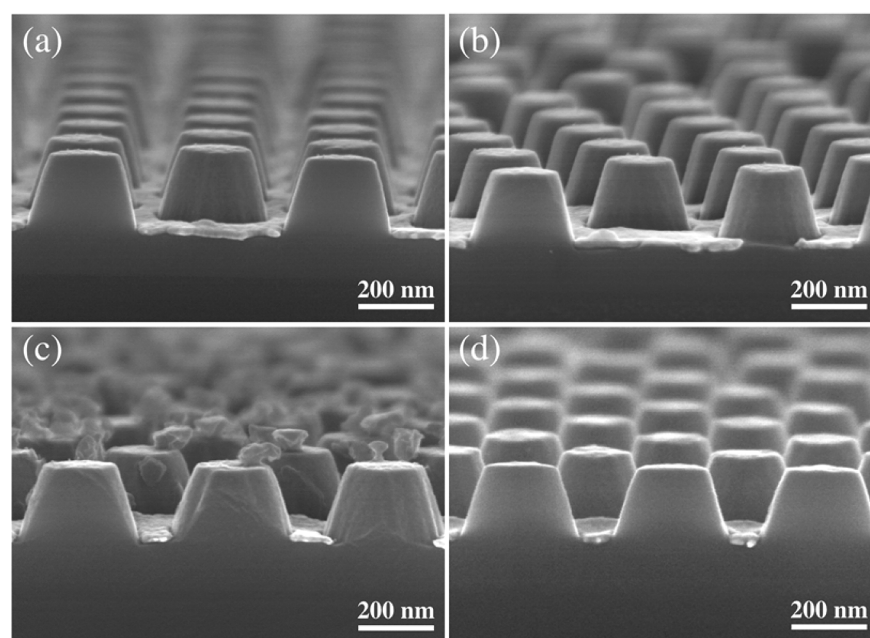

Figure 5. Cross-section SEM micrographs of $In_{0.53}Ga_{0.47}As$ pillars after digital etching. (a) A pillar array produced by 5 min MacEtch in a solution of 14.2 M HF and 5.3 mM $KMnO_4$ after 1 cycle of digital etching showing smooth sidewalls. (b) The same sample as in (a) but after 2 cycles of digital etching, showing negligible changes in the diameter from (a). (c) A pillar array produced by 7 min MacEtch in a solution of 14.2 M HF and 3.2 mM $KMnO_4$ after 1 cycle of digital etching showing sidewall roughness and residuals. (d) The same sample as in (c) but after 2 cycles of digital etching showing smooth sidewalls.

not significant.[29] Furthermore, as analyzed in Figure S8 and shown Figure 4d, the valence bands of GaAs, $In_{0.53}Ga_{0.47}As$, and InAs are well above the redox potential of $KMnO_4$ (1.51 V *vs* the standard hydrogen electrode potential, V_{SHE}), suggesting that the variation in band energy position is not sufficient to affect the charge transfer and is not the governing factor either.

Porous Shell Removal with Digital Etching. Recently, ultra-high aspect ratio InP FinFETs, fabricated using MacEtch, have been demonstrated with excellent performance.[12] The success was attributed to the nature of inverse MacEtch that provides extremely smooth sidewalls on InP fins.[11] On the other hand, the traditional forward MacEtch on Si or GaAs, *etc.*, suffers from sidewall morphology issues resulting from the metal catalyst edge roughness or the formation of a porous shell.[4,9,13,16] It is obvious that in order to use the MacEtch $In_{0.53}Ga_{0.47}As$ pillar array for electronic and optoelectronic device applications, the porous shell must be removed, as the porosity on the pillar sidewalls and surfaces will degrade the electrical performance detrimentally. A general approach is required to solve the sidewall roughness issues associated with MacEtch catalyst edge roughness or chemical etch-induced porosity.

Digital etching is a wet etching technique to isotropically remove the surface of compound semiconductors a few nanometers at a time.[34,36,49] This process includes oxidation and oxide removal etching steps that are performed alternately. Since it is a self-limiting etching process, the thickness of removed material can be precisely controlled by the number of cycles employed. This technique has been widely used to improve the surface quality of compound semiconductors. For example, $In_xGa_{1-x}As$ nanowire MOSFETs[36] and InAs planar nanowire gate-all-around MOSFETs,[49] with impressive performance after multiple cycles of digital etching, were demonstrated. In this work, we found that the porous shell on the sidewalls of $In_{0.53}Ga_{0.47}As$ pillars can be efficiently removed by digital etching. Depending on the porosity, one or two cycles of digital etching are sufficient for full removal of the $In_{0.53}Ga_{0.47}As$ porous layer to expose the solid $In_{0.53}Ga_{0.47}As$ core. The digital etching results of $In_{0.53}Ga_{0.47}As$ pillars produced in a MacEtch solution of 14.2 M HF and 5.3 mM $KMnO_4$ (Figure 3d) are shown in Figure 5a,b. It can be seen that the porous shell is completely removed, leaving the pillars with extremely smooth sidewalls. It is worth noting that the porous layer is nearly ~50 nm thick. The complete removal of the thick porous structure in one cycle of digital etching indicates the high porosity of the $In_{0.53}Ga_{0.47}As$ shell. To confirm the full removal of the porous shell, the second cycle of digital etching is performed, and the morphology of $In_{0.53}Ga_{0.47}As$ pillar is examined in Figure 5b. Negligible change in the pillar diameter between the first and second cycles suggests that the porous layer has been completely removed, and further digital etching only removes several nanometers thick of the $In_{0.53}Ga_{0.47}As$ solid core.

As mentioned above, the oxidation and oxide removal rate for the $In_{0.53}Ga_{0.47}As$ porous structure is reliant on its porosity. For $In_{0.53}Ga_{0.47}As$ pillars with low porosity shells which can be formed from MacEtching under extremely low oxidant MacEtch condition, more cycles of digital etching may be necessary to produce smooth sidewalls. For the sample shown in Figure S5b, it was found that there are plenty of residuals left either on the top or on the sidewall of the pillars after one cycle of digital etching (Figure 5c). This is because the porosity is low under this etching condition, and thus the surface area exposed to the oxygen source is small, leading to a slower oxidation rate. Therefore, to remove the porous shell with lower porosity, two or even more cycles of digital etching must be performed, as demonstrated in Figure 5d. We can conclude that the digital etching not only removes the porous structure and surface roughness on MacEtched $In_{0.53}Ga_{0.47}As$ pillars but also has the capability to characterize the porosity of

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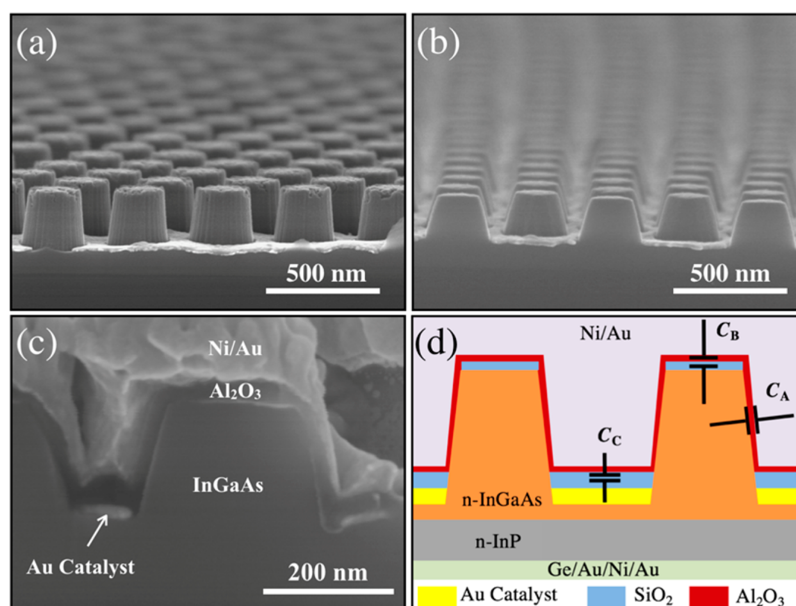

Figure 6. Cross-section SEM micrographs showing the main steps of process flow in the fabrication of $In_{0.53}Ga_{0.47}As$ pillar array MOSCAPs. (a) Array of $In_{0.53}Ga_{0.47}As$ pillars produced by MacEtch. (b) Array of $In_{0.53}Ga_{0.47}As$ pillars with smooth sidewalls after digital etching. (c) High-magnification cross-section view of a fully fabricated $In_{0.53}Ga_{0.47}As$ pillar array MOSCAP with Al_2O_3 high-*k* dielectric and Ni/Au metal gate. (d) Schematic illustration of the cross-section of $In_{0.53}Ga_{0.47}As$ pillar MOSCAP and the representation of three capacitance components.

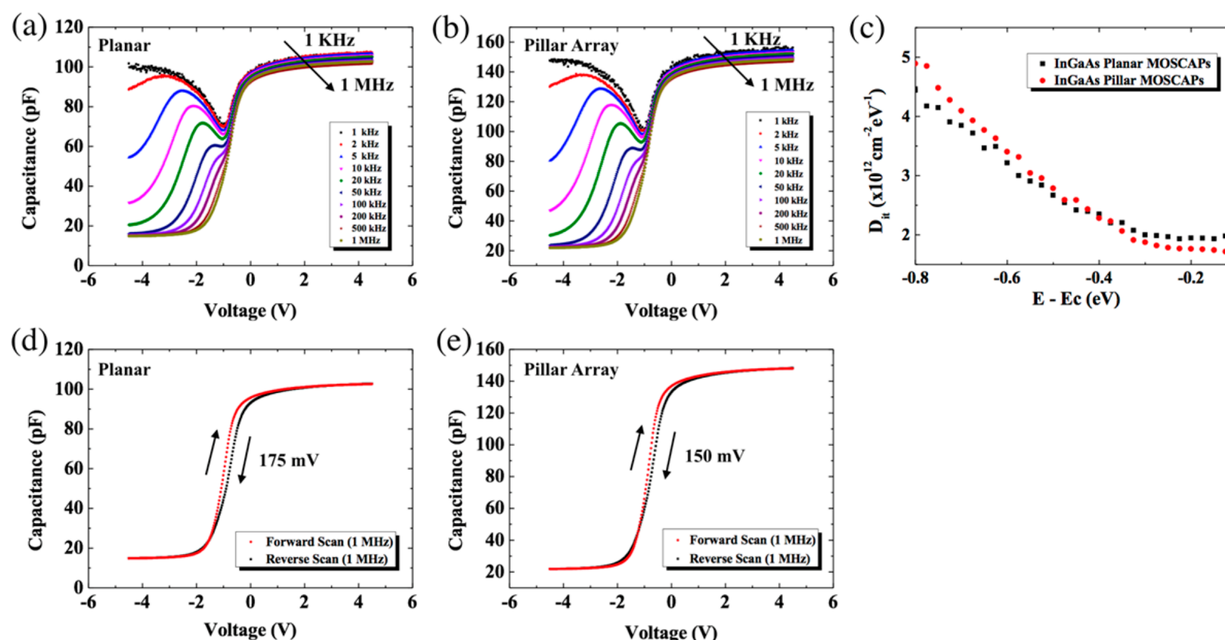

Figure 7. Room-temperature multifrequency *C*−*V* curves of (a) $In_{0.53}Ga_{0.47}As$ planar MOSCAP and (b) $In_{0.53}Ga_{0.47}As$ pillar array MOSCAP. (c) D_{it} *versus* position in the bandgap with respect to the conduction band for both types of $In_{0.53}Ga_{0.47}As$ MOSCAPs extracted using the high- (1 MHz) and low-frequency (2 kHz) methods. Bidirectional hysteresis *C*−*V* responses of (d) the $In_{0.53}Ga_{0.47}As$ planar MOSCAP and (e) $In_{0.53}Ga_{0.47}As$ pillar MOSCAP at 1 MHz and room temperature.

nanostructures etched under different etching conditions through the minimum number of cycles of digital etching required to produce smooth surface.

$In_{0.53}Ga_{0.47}As$ Pillars Array MOSCAPs for Surface Quality Characterization. The quality of the compound semiconductor (*i.e.*, GaAs, $In_{0.53}Ga_{0.47}As$, *etc.*) surface is one of the most crucial factors that determines the performance of electronic devices such as MOSFETs.[29,30] To confirm and further evaluate the surface quality of the etched $In_{0.53}Ga_{0.47}As$ nanostructures previously shown by SEM, metal-oxide-semiconductor capacitors (MOSCAPs) were fabricated. The MOSCAP is an effective structure for surface quality characterization that has been successfully employed for many different compound semiconductors, for example, $In_{0.53}Ga_{0.47}As$ and InAs, *etc.*[50,51] Here we fabricate MOSCAPs on both MacEtched $In_{0.53}Ga_{0.47}As$ pillars and planar $In_{0.53}Ga_{0.47}As$ film (to act as a control structure). This allows us to examine the surface quality through a quantitative comparison of the resultant interface state density (D_{it}) extracted from capacitance−voltage (*C*−*V*) measurements.

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Figure 6a–c shows the cross-section SEM images of the main fabrication steps for $In_{0.53}Ga_{0.47}As$ pillar array MOSCAPs, and the corresponding schematic cross-section of the completed MOSCAPs is illustrated in Figure 6d. Briefly, ordered $In_{0.53}Ga_{0.47}As$ pillars were first produced by MacEtch (Figure 6a). Subsequently, a porosity removal step was performed by digital etching (Figure 6b). After isolating the Au catalyst with evaporated SiO_2 and passivating the exposed $In_{0.53}Ga_{0.47}As$ pillar surfaces by dilute ammonium sulfide $(NH_4)_2S$ solution, a thin layer (~20 nm) of Al_2O_3 gate dielectric was deposited and then annealed for 30 s at 300 °C in a N_2 environment. To provide conformal gate metal coverage of pillar sidewalls, Ni/Au gate metal was sputtered (Figure 6c). Ge/Au/Ni/Au was subsequently evaporated on the backside of the sample, followed by RTA in N_2 at 300 °C for 30 s to form back ohmic contact to the n^+ InP substrate. The schematic illustration of the cross-section of the completed $In_{0.53}Ga_{0.47}As$ pillars MOSCAPs is shown in Figure 6d.

Figures 7a,b shows the $C-V$ response at room temperature, with ac signal frequencies varied from 1 kHz to 1 MHz, for the $In_{0.53}Ga_{0.47}As$ planar and MacEtched pillar MOSCAPs as a function of the metal gate voltage that was varied from −4.5 to 4.5 V. The gate metal pads patterned on both MOSCAPs have the same area of 4.41×10^{-4} cm^2, that is, one pillar MOSCAP device consists of roughly 2.9×10^5 $In_{0.53}Ga_{0.47}As$ pillars. However, due to the low aspect ratio, there is not much difference in the $In_{0.53}Ga_{0.47}As$ pillar total surface area as compared to the planar device. The total capacitance (C_{total}) of the pillar MOSCAPs structure consists of three components that are connected in parallel, as shown in Figure 6d. The first one is the capacitance of the pillar MOSCAPs at the pillar sidewall (C_A), the second one is the capacitance of the pillar MOSCAP at the pillar top (C_B), and the third one is the capacitance of the gate metal/oxide (high-k Al_2O_3 and SiO_2)/catalyst metal (MIM) structure (C_C). Since C_C is nearly eight times smaller and does not vary with frequency change, the presence of C_C, which simply adds to the measured total capacitance, does not affect the frequency dependent $C-V$ characteristics. The measured capacitance of pillar MOSCAPs from inversion to accumulation is roughly 1.5 times larger than planar MOSCAPs, which is consistent with the calculated values (Supporting Information S9).

As shown in Figure 7a,b, the $C-V$ curves of planar and pillar $In_{0.53}Ga_{0.47}As$ MOSCAPs show saturation to an oxide capacitance of ~100 pF and 150 pF, respectively. It can be observed that both types of MOSCAPs exhibit similar $C-V$ characteristics, including frequency dispersion in accumulation, $C-V$ stretch-out in depletion, and large capacitance difference at inversion. First, it is noted that both types of MOSCAP devices exhibit relatively high negative flat band voltage (V_{FB}) and threshold voltage (V_T), which probably result from a combination of nonoptimized gate metal work function and fixed oxide charges in the high-k Al_2O_3 dielectric. Similar observation of negative shift in V_T was reported in other work.[12] Second, it can be observed that the maximum capacitance at the accumulation region decreases as the ac frequency increases and appears to saturate at the highest frequency (1 MHz). This frequency dispersion, depending on the severity (~5–23%), is typically attributed to the tunneling of carriers between the substrate and border traps (defect states) in the high-k Al_2O_3 dielectric, which cannot respond quickly enough to a high-frequency ac voltage signal and thus "freeze out" with increasing frequency[51−54] or interface traps.[55] In contrast, the frequency dispersion at the accumulation region, from a similar measurement frequency range for both types of MOSCAPs in this work, is only ~2.4%. Such small dispersion probably results from the $In_{0.53}Ga_{0.47}As$ surface passivation in dilute $(NH_4)_2S$ solution before dielectric deposition and post-dielectric deposition annealing.[51−53]

The observation of increased low-frequency capacitance in depletion ($C-V$ stretch-out) and the large capacitance difference in inversion are attributed to frequency-dependent interface states. In this work, the extraction of the interface state density (D_{it}) was performed using the high- and low-frequency $C-V$ technique,[51,56−59] which is known to be a straightforward and robust approach to estimate the D_{it}. Other D_{it} extraction techniques, such as, Terman's or conductance methods, are also used in literature.[51−53,56] However, those methods are sensitive to various factors, such as the uniformity of dopant concentration, oxide capacitance, possible high D_{it} at the high-k dielectric and compound semiconductor interface, and the presence of the weak inversion response for narrow bandgap semiconductors.[56,60] At low frequency, the interface traps have time to respond to the slowly changing ac signal and therefore add a capacitance to the measured low-frequency $C-V$ curve, denoted as C_{LF}. Here, the C_{LF} was chosen at a frequency of 2 kHz at room temperature. In contrast, at high frequencies, interface defect states cannot respond to the ac signal fast enough, and therefore they contribute little or no capacitance to the high-frequency $C-V$ measurement, denoted by C_{HF}. Here, C_{HF} was taken at 1 MHz. The capacitance associated with the interface states can be extracted using eq 1, and the D_{it} estimation is obtained using eq 2 as shown below:

$$C_{it} = \left(\frac{1}{C_{LF}} - \frac{1}{C_{ox}}\right)^{-1} - \left(\frac{1}{C_{HF}} - \frac{1}{C_{ox}}\right)^{-1} \quad (1)$$

$$D_{it} = \frac{C_{it}}{q} \quad (2)$$

It is worth mentioning that in the case of interface defects with a discrete energy level in the bandgap, the $C-V$ curve of n-type $In_{0.53}Ga_{0.47}As$ at low frequency is expected to go through a peak (observed in the $C-V$ curve at a frequency above 2 kHz but below 200 kHz) at inversion (negative gate bias). Thus, the D_{it} extraction using the high–low-frequency method will work more effectively if the C_{LF} curve with a peak at inversion is chosen.[51−53,57] In contrast, the monotonic increase of capacitance in inversion at decreasing frequency could be attributed either to the response of minority carriers or to the presence of interface states deep within the bandgap.[51] In this work, the lowest frequency to exhibit the interface defects related response that passes through a peak is 2 kHz. Thus, the $C-V$ curve measured at 2 kHz was chosen as C_{LF} for D_{it} extraction in this study. In the case of the 1 kHz $C-V$ curve, it is difficult to distinguish the contribution of either interface defects or minority carriers, owing to the presence of significant measurement noises. Therefore, C_{LF} was chosen to be 2 kHz as it is the minimum frequency that can be relied on in the $C-V$ measurement.

Even though the D_{it} extracted using the high- and low-frequency method represents a lower bound to the true D_{it} value, these $C-V$ curves are still very useful for a comparative evaluation of the D_{it} for both pillar and planar $In_{0.53}Ga_{0.47}As$ MOSCAPs that were fabricated using the same process flow.[56−58] Thus, it is a good parameter to examine whether

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the MacEtch technique is capable of fabricating $In_{0.53}Ga_{0.47}As$ nanostructures with smooth sidewalls for device application. The plots of D_{it} versus position in the bandgap with respected to the conduction band for both types of MOSCAPs are shown in Figure 7c. It can be seen that the midgap D_{it} (at around −0.37 eV with respect to the bottom of the conduction band) of the two types of MOSCAPs is comparable at ∼1.9−2.2 × 10^{12} cm^{-2} eV^{-1}. It is worth noting that the midgap D_{it} extracted in this work for both types of $In_{0.53}Ga_{0.47}As$ MOSCAPs is similar as compared to other reports.[51,52,59] Even though the fabrication conditions of the MOSCAP devices in this work are not fully optimized (*e.g.*, the D_{it} could be further improved with optimized pillar size, spacing, and height, forming gas annealing and better metal contact), the experimental demonstration of comparable D_{it} for both types of $In_{0.53}Ga_{0.47}As$ MOSCAPs provides strong evidence that the surface of $In_{0.53}Ga_{0.47}As$ after MacEtch is free of damages and roughness from etching, which is a significant improvement as compared to traditional RIE.

Furthermore, the room-temperature, high-frequency (1 MHz) $C-V$ hysteresis responses of the pillar and planar $In_{0.53}Ga_{0.47}As$ MOSCAPs were obtained for comparison, as shown in Figure 7d,e, respectively. The $C-V$ measurement starts from inversion and the gate voltage sweeps toward accumulation (forward) and then subsequently sweeps back toward inversion (reverse). The $C-V$ hysteresis, that is, the gate voltage difference between the bidirectional scan, is estimated at the flat-band capacitance. It can be seen that the $C-V$ curve shifts toward positive voltage during the reverse scan, suggesting that negative charge trapping or positive charge detrapping is occurring through the interface states.[61] The evidence of comparable hysteresis of ∼150−175 mV, exhibited in the $C-V$ measurements of both types of MOSCAPs, further confirms that the MacEtch is capable of fabricating $In_{0.53}Ga_{0.47}As$ nanostructures with smooth surfaces for device application.

CONCLUSION

In conclusion, we have reported the successful demonstration of MacEtch of ternary compound semiconductor $In_{0.53}Ga_{0.47}As$, producing ordered, uniform, array-based $In_{0.53}Ga_{0.47}As$ pillars with diameters as small as 200 nm and surfaces with excellent quality. The vertical etch rate increases as a function of oxidant concentration. By tuning the acid, oxidant, and DI water concentration, the competition between mass and charge transport can be varied such that pillar morphologies including the porous shell thickness can be manipulated. However, owing to the low Schottky barrier height between the Au catalyst and $In_{0.53}Ga_{0.47}As$, the etching mechanism is confined in the mass transport limited regime, where the formation of a porous layer is difficult to avoid. An optimized digital etching process was developed to facilitate the complete removal of the porous layer and other surface roughness. Remarkably, the evidence of comparable midgap interface state density and flat-band capacitance hysteresis of both planar and pillar $In_{0.53}Ga_{0.47}As$ MOSCAPs further demonstrates that the sidewalls of the resultant pillars from MacEtch are smooth and free of porosity and damages. This method offers a simple, room-temperature, and low-cost technique for the formation of the technologically important $In_{0.53}Ga_{0.47}As$ nanostructures with high quality side-walls. On the fundamental side, the etching mechanism uncovered will provide insights in furthering the versatilities of MacEtch application in other types of compound semi-conductors as well. We believe this work represents a significant advancement in pushing MacEtch toward a critically important frontier and will be of great value for electronic and photoelectronic device applications, including nanoscale high-mobility field-effect transistors, photovoltaics, lasers, and infrared detectors.

EXPERIMENTAL METHODS

Growth of $In_{0.53}Ga_{0.47}As$ Epitaxial Film on InP (100) Substrates. The unintentionally doped $In_{0.53}Ga_{0.47}As$ was epitaxially grown using a close coupled showerhead (CCS) Aixtron metal organic chemical vapor deposition (MOCVD) reactor. An epi ready (100)-oriented n^+ InP substrate (AXT, Inc.) was used for the growth. The growth pressure was kept at 100 mbar. The substrate was first baked at 650 °C in phosphine (PH_3) overpressure with a flow rate of 100 sccm. Following this, 200 nm-thick InP buffer was grown at 610 °C with 200 sccm of PH_3 and two trimethyl indium (TMIn) lines with flow rates of 250 and 125 sccm, respectively. Next, a 500 nm-thick $In_{0.53}Ga_{0.47}As$ layer was grown with 15 sccm of trimethyl gallium (TMGa) diluted with 100 sccm of hydrogen (effective flow rate of TMGa was 4.2 sccm), 50 sccm arsine (AsH_3), and the two TMIn lines with equivalent flow rates of 125 sccm. The background doping concentration of the $In_{0.53}Ga_{0.47}As$ film grown under identical condition but on a semi-insulating InP substrate was found to be ∼3 × 10^{16} cm^{-3} by Hall effect measurement.

Fabrication of $In_{0.53}Ga_{0.47}As$ Pillar Array by MacEtch. The as-grown $In_{0.53}Ga_{0.47}As$ samples were first precleaned in acetone, isopropyl alcohol (IPA), and DI water for 5 min each, followed by drying under nitrogen (N_2) gun. Subsequently, the sample was coated with a hexagonal close-packed monolayer of colloidal polystyrene nanospheres with nominal diameter of ∼290 or 390 nm (Bang laboratories, Inc.) by using the air/water interface method.[62] Subsequently, the nanospheres were trimmed to smaller diameter of ∼180 or 300 nm (±20 nm), respectively, in the FEMTO oxygen (O_2) plasma cleaner. Using the resized nanospheres as a blocking mask, Au catalyst with nominal thickness of 20 nm (±2 nm) was evaporated onto the $In_{0.53}Ga_{0.47}As$ sample using the CHA SEC-600 electron beam evaporator operating under a chamber pressure of 1 × 10^{-6} Torr. The Au thickness was measured *in situ* by a quartz crystal microbalance. Subsequently, the nanospheres were lifted off by ultrasonication in IPA for 1 min, which left a hexagonally ordered Au nanomesh pattern with diameter of ∼180 or 300 nm (±20 nm) and spacing of 100 nm for MacEtch. The catalytic etching was conducted in a dark environment, and the etching solution consisted of different concentrations of hydrofluoric acid (HF), varied from 4.7 to 23.7 M, and potassium permanganate ($KMnO_4$), varied from 2.1 to 21.1 mM, at room temperature for a duration of 2.5 to 10 min, depending on the experimental requirements. After the etching process was completed, the samples were gently rinsed in DI water before drying by N_2 gun. In this work, the total volume of etching solution was kept constant for all experiments. The fabricated $In_{0.53}Ga_{0.47}As$ pillars were examined by a high-resolution scanning electron microscope (SEM, Hitachi S4800). The vertical etch rate was computed from the height of $In_{0.53}Ga_{0.47}As$ pillars divided by the etching duration, assuming the etch rate was constant during the MacEtch process. The porous $In_{0.53}Ga_{0.47}As$ shell formed during MacEtch was removed by isotropic digital etching, where oxidation (at room temperature in a UV ozone cleaner from Bio Force Nanoscience, Inc.) and oxide removal etching (by dilute HF) were performed alternately. Depending on the porosity of the porous $In_{0.53}Ga_{0.47}As$ shell, one or two cycles of digital etching were employed for full removal of the $In_{0.53}Ga_{0.47}As$ porous layer to expose the $In_{0.53}Ga_{0.47}As$ solid core. This method could reveal the distribution of the porous $In_{0.53}Ga_{0.47}As$ layer under different etching conditions for process optimization to achieve $In_{0.53}Ga_{0.47}As$ pillars with controllable sidewalls. Importantly, the sidewall surface grooves induced by the catalyst pattern edge roughness duirng MacEtch can also be alleviated.

$In_{0.53}Ga_{0.47}As$ Pillar Array MOSCAPs Fabrication and Characterization. The ordered $In_{0.53}Ga_{0.47}As$ pillar array, with pillar height of ∼180 nm and diameter of ∼290 nm, was fabricated by MacEtch in optimized condition using Au-catalyst patterned by ∼390 nm

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nanospheres lithography. The undesired grooves on both the top and sidewalls of the pillars were completely removed using digital etching. The Au catalyst film was passivated by ~100 nm-thick silicon dioxide (SiO_2), and subsequently, dilute HF etch back was performed to remove excess SiO_2 on the sidewalls of the pillars, which left ~20 nm SiO_2 on top of the Au catalyst. $In_{0.53}Ga_{0.47}As$ pillar surface passivation was performed in dilute ($(NH_4)_2S$) solution. The samples were then immediately loaded into an atomic layer deposition (ALD) chamber for aluminum oxide (Al_2O_3) gate dielectric (~20 nm thick) deposition, followed by a 30 s of RTA at 300 °C in N_2 environment. To provide conformal gate metal coverage of the pillars sidewalls, sputtering of nickel/gold (Ni/Au) gate metal was employed. Ge/Au/Ni/Au was subsequently evaporated at the backside of samples, followed by RTA in N_2 at 300 °C for 30 s to form ohmic contacts. The *C*−*V* response at room temperature, with ac signal frequency varied from 1 kHz to 1 MHz, for $In_{0.53}Ga_{0.47}As$ planar and pillar MOSCAPs, was measured by a probe station that was connected to the Keithley 4200 parameter analyzer.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsnano.7b04752.

> Sidewall profile of over-etched $In_{0.53}Ga_{0.47}As$ pillars; evolution of $In_{0.53}Ga_{0.47}As$ pillars profiles as a function of HF concentration; evolution of $In_{0.53}Ga_{0.47}As$ pillars profiles as a function of $KMnO_4$ concentration; evolution of porous region ratio as a function of etch duration; effect of $KMnO_4$ concentration on porosity of MacEtched $In_{0.53}Ga_{0.47}As$ pillars; effect of temperature on porosity of MacEtched $In_{0.53}Ga_{0.47}As$ pillars; MacEtch results of GaAs with identical condition as $In_{0.53}Ga_{0.47}As$; mapping of GaAs, $In_{0.53}Ga_{0.47}As$ and InAs bandgap energy with redox potential of $KMnO_4$; capacitance of $In_{0.53}Ga_{0.47}As$ pillar and planar MOSCAPs calculation (PDF)

AUTHOR INFORMATION

Corresponding Author

*E-mail: xiuling@illinois.edu.

ORCID

Lingyu Kong: 0000-0001-6057-8144

Sing Yang Chiam: 0000-0002-5157-3533

Present Addresses

[∇]IBM Thomas J. Watson Research Center, 257 Fuller Road, Albany, New York, 12206, United States

[○]Department of Electrical and Computer Engineering, Microelectronics Research Center, University of Texas at Austin, Austin, Texas, 78705, United States

Author Contributions

L.Y.K. performed all experiments. L.Y.K. and X.L. designed the experiment, performed data analysis, and wrote the manuscript. L.Y.K. and Y.S. designed the MOSCAPs fabrication flow and analyzed the *C*−*V* data. J.D.K. grew the $In_{0.53}Ga_{0.47}As$ wafers and assisted in developing the etching recipes at the initial stage. X.L. supervised the project. All the authors discussed the data and commented on the manuscript.

Notes

The authors declare no competing financial interest.

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